TOSHIBA GTR Module Silicon N Channel IGBT

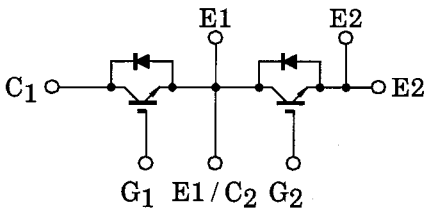
MG75J2YS50

High Power Switching Applications

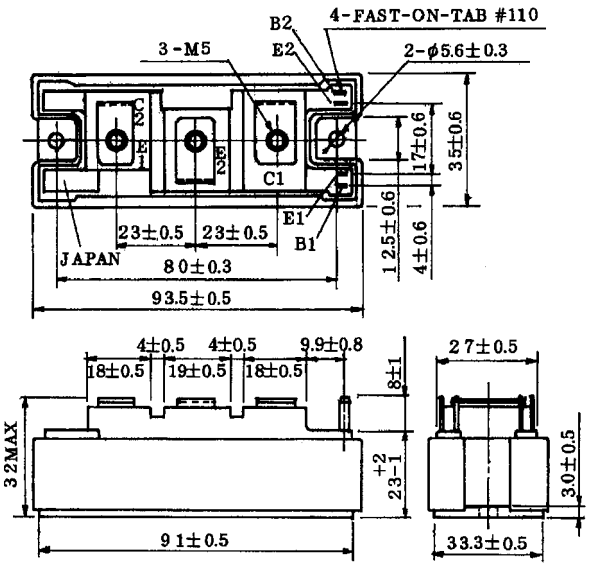
Motor Control Applications

- The electrodes are isolated from case.
- High input impedance.
- Includes a complete half bridge in one package.
- Enhancement-mode.
- High speed : t_f = 0.30μs(Max) (I_C = 75A)
  t_{rr} = 0.15μs(Max) (I_F = 75A)
- Low saturation voltage
  : $V_{CE\ (sat)}$ = 2.70V (Max) (I_C = 75A)

Equivalent Circuit



Unit: mm



JEDEC	—
EIAJ	—
TOSHIBA	2-94D1A

Weight: 202g (Typ.)

Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Collector-emitter voltage		V_{CES}	600	V
Gate-emitter voltage		V_{GES}	±20	V
Collector current	DC	I_C	75	A
	1ms	I_{CP}	150	
Forward current	DC	I_F	75	A
	1ms	I_{FM}	150	
Collector power dissipation (T_c = 25°C)		P_C	390	W
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−40 ~ 125	°C
Isolation voltage		V_{Isol}	2500 (AC 1 min.)	V
Screw torque (Terminal / mounting)		—	3 / 3	N·m

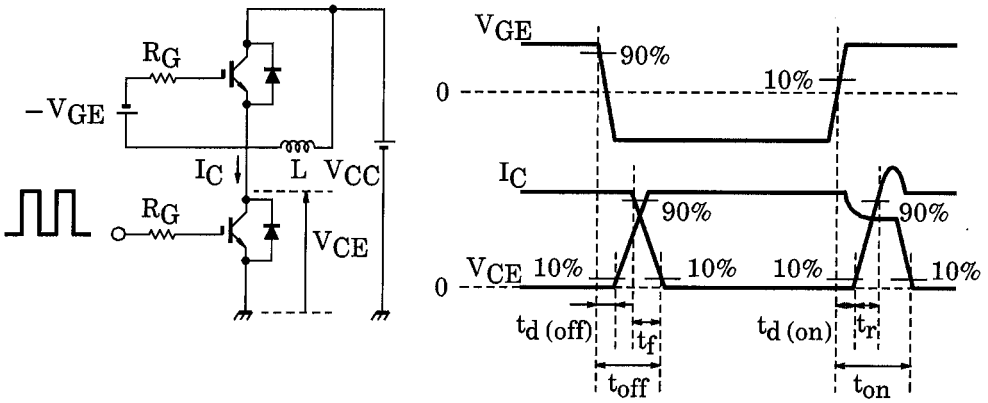
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Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GES}	V_{GE} = ±20V, V_{CE} = 0	—	—	±500	nA
Collector cut-off current		I_{CES}	V_{CE} = 600V, V_{GE} = 0	—	—	1.0	mA
Gate-emitter cut-off voltage		$V_{GE\ (off)}$	I_C = 7.5mA, V_{CE} = 5V	5.0	7.0	8.0	V
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = 75A, V_{GE} = 15V	—	2.10	2.70	V
Input capacitance		C_{ies}	V_{CE} = 10V, V_{GE} = 0, f = 1MHz	—	7100	—	pF
Switching time	Turn-on delay time	$t_{d\ (on)}$	Inductive load V_{CC} = 300V I_C = 75A V_{GE} = ±15V R_G = 18Ω (Note 1)	—	0.08	0.16	μs
	Rise time	t_r		—	0.12	0.24	
	Turn-on time	t_{on}		—	0.40	0.80	
	Turn-off delay time	$t_{d\ (off)}$		—	0.20	0.40	
	Fall time	t_f		—	0.15	0.30	
	Turn-off time	t_{off}		—	0.50	1.00	
Forward voltage		V_F	I_F = 75A, V_{GE} = 0	—	2.10	2.80	V
Reverse recovery time		t_{rr}	I_F = 75A, V_{GE} = −10V di / dt = 100A / μs	—	0.08	0.15	μs
Thermal resistance		$R_{th\ (j-c)}$	Transistor stage	—	—	0.32	°C / W
			Diode stage	—	—	0.69	

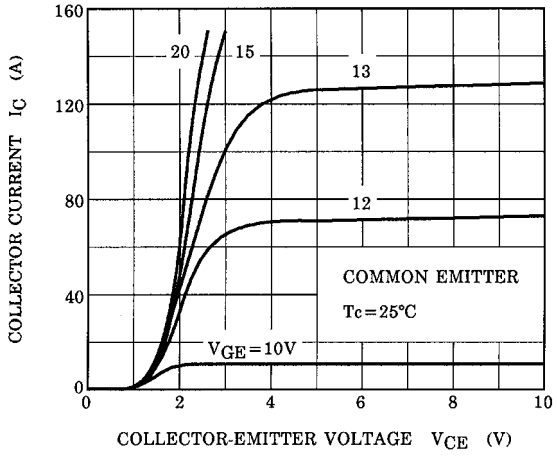
Note 1: Switching time test circuit & timing chart



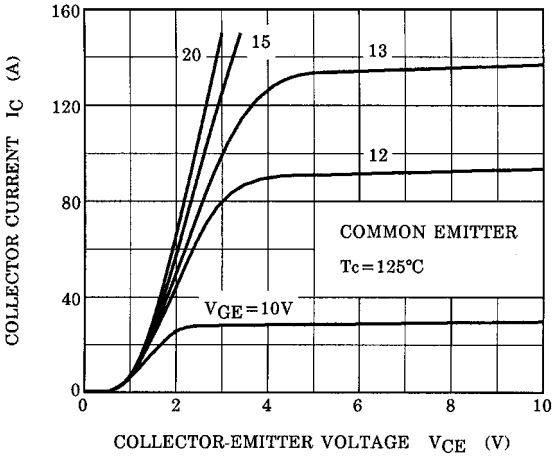
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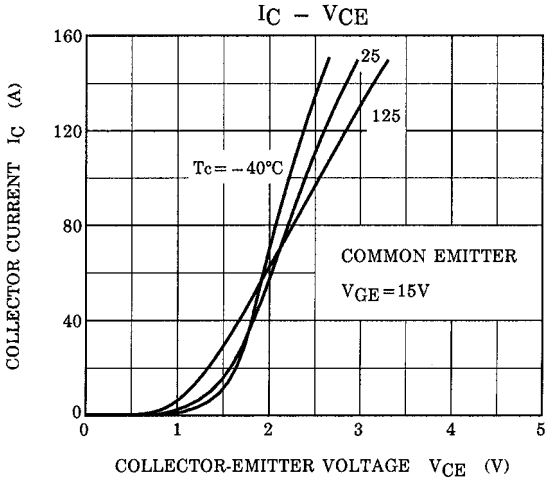
I_C – V_{CE}



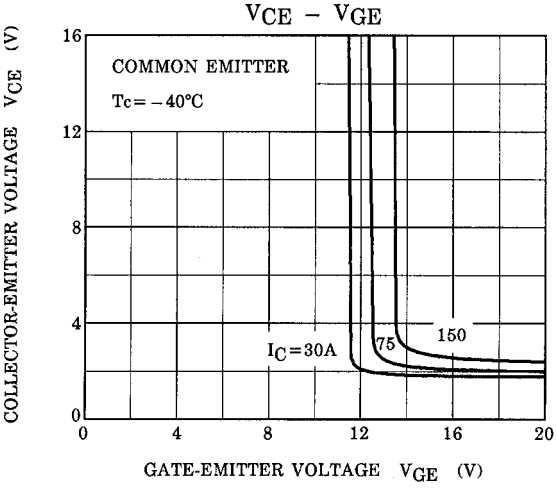
I_C – V_{CE}



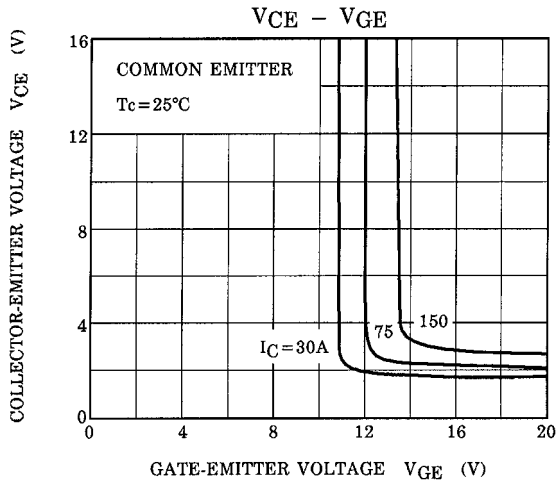
I_C – V_{CE}



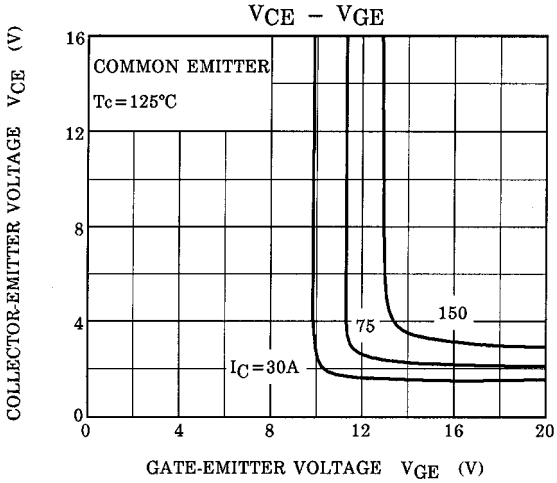
V_{CE} – V_{GE}



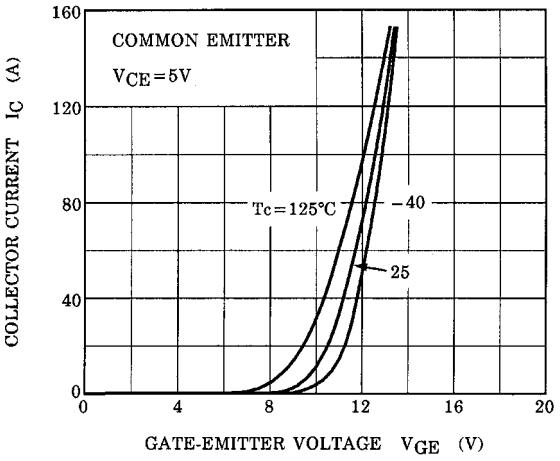
V_{CE} – V_{GE}



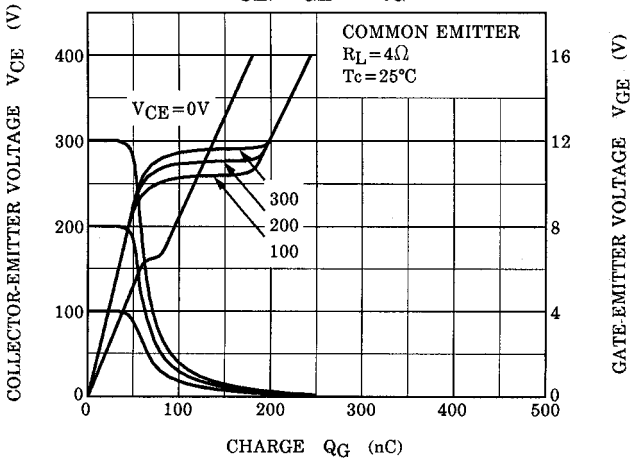
V_{CE} – V_{GE}



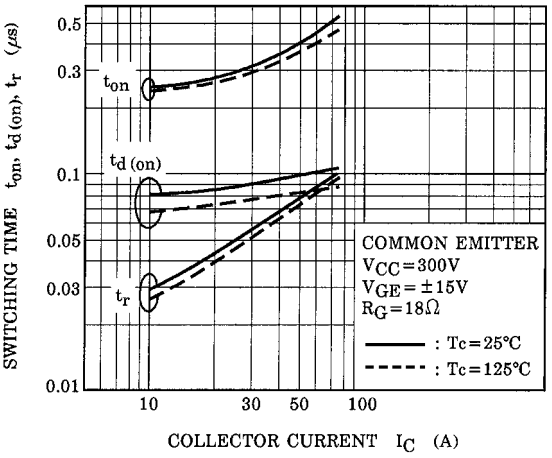
I_C – V_{GE}



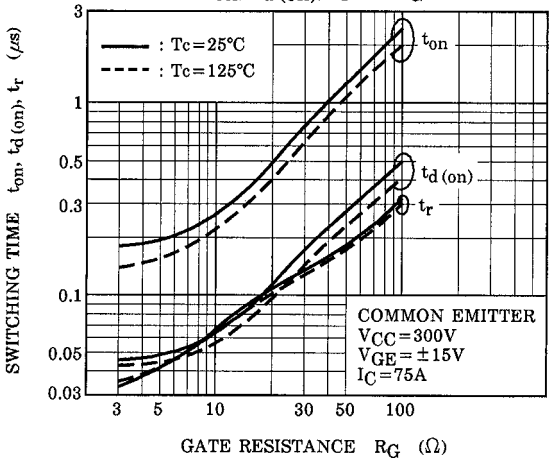
V_{CE}, V_{GE} – Q_G



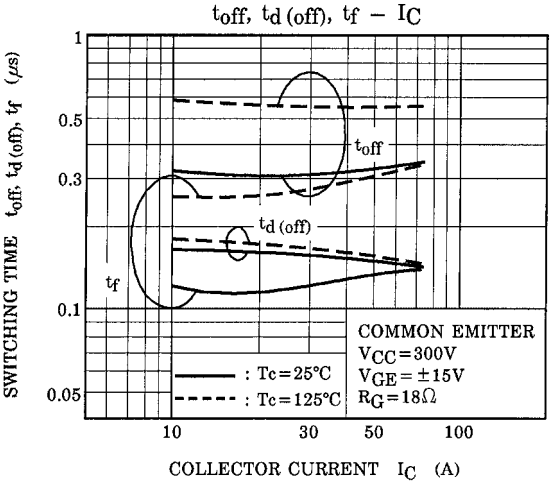
t_{on}, $t_{d\,(on)}$, t_r – I_C



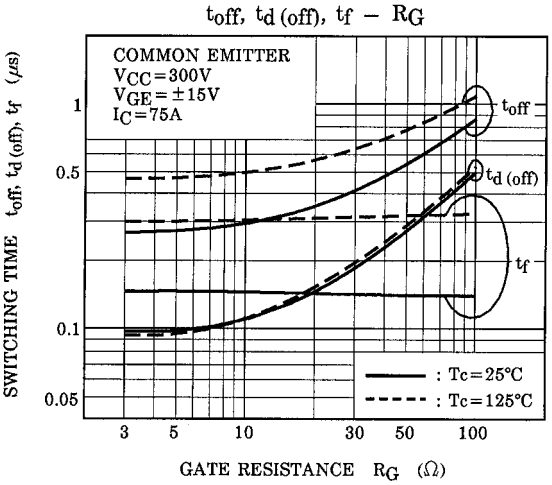
t_{on}, $t_{d\,(on)}$, t_r – R_G



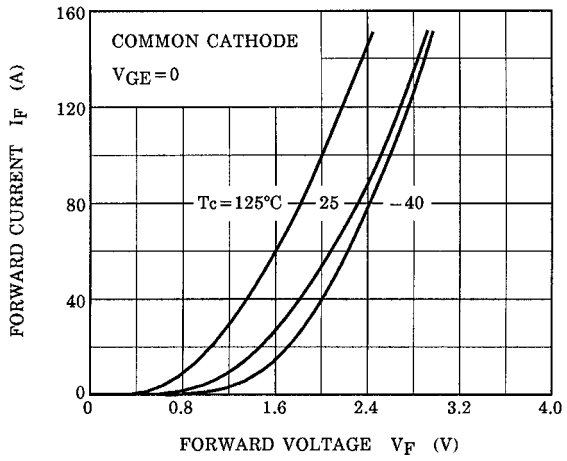
t_{off}, $t_{d\,(off)}$, t_f – I_C



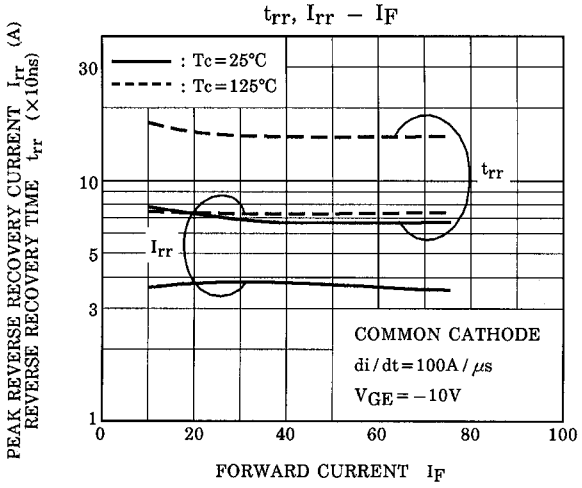
t_{off}, $t_{d\,(off)}$, t_f – R_G



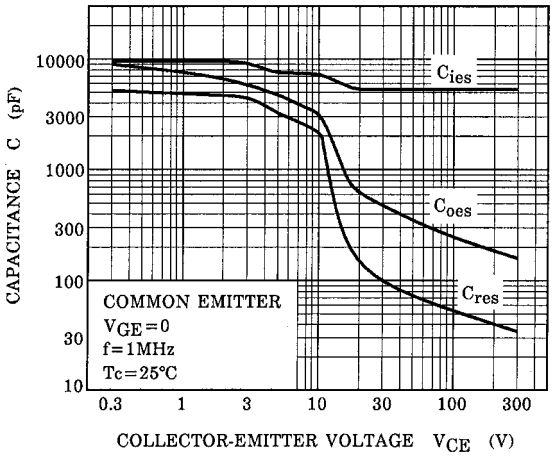
$I_F - V_F$



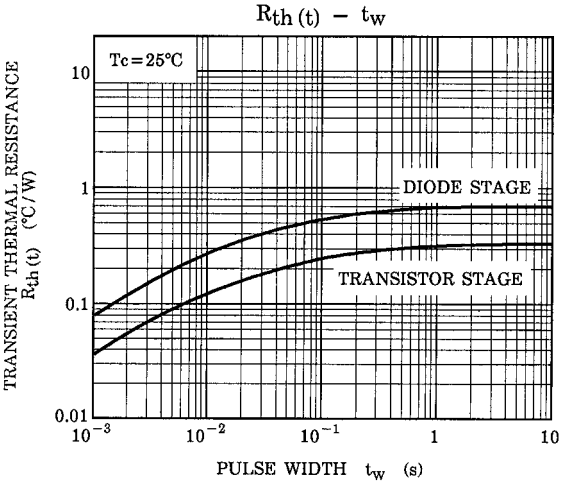
$t_{rr}, I_{rr} - I_F$



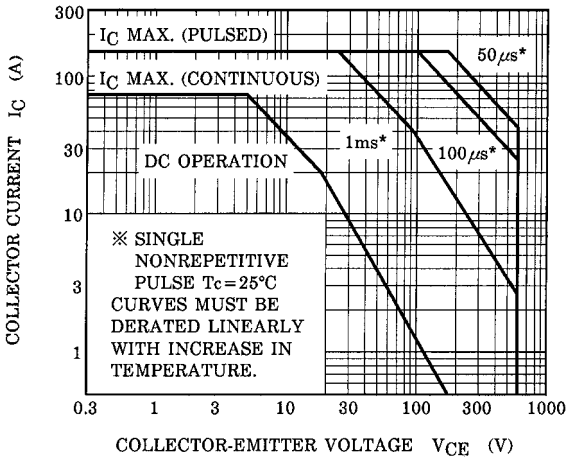
$C - V_{CE}$



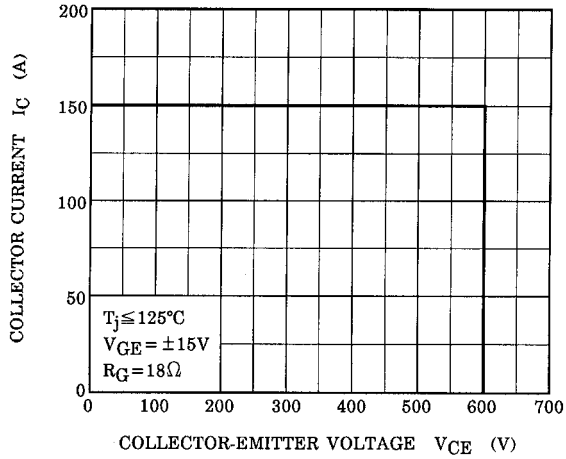
$R_{th}(t) - t_w$



SAFE OPERATING AREA



REVERSE BIAS SOA



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